Method For Testing Embedded DRAM Arrays

Abstract of the Disclosure

A method and system for testing a DRAM comprised of DRAM blocks. The method comprises: in a processor based built-in self test system, generating a test data pattern; for each DRAM block, performing a write of the test data pattern into the DRAM block, performing a pause for a predetermined period of time, and performing a read of a resulting data pattern from the DRAM block; wherein for each DRAM block, the performing the write of the test pattern into the DRAM block is performed before the performing the pause for the predetermined period of time, and the performing the read of the resulting data pattern from the DRAM block is performed after the performing the pause for the predetermined period of time; and wherein at least a portion of the pause for the predetermined period of time of two or more the DRAM blocks overlap in time.

Figures